Abstract of the Disclosure:

A circuit configuration for reading out a programmable link enables programming the programmable link in addition to reading out the programmed value into a volatile memory cell. For this purpose, address lines that are present are coupled to the input of the volatile memory cell by additional switches. Given the presence of a hit signal at the output of a combination unit, the switches are driven by a control circuit in a manner dependent on a set signal. The present circuit is particularly suitable for dynamic semiconductor memories and for mass production.

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